



FDMC6890NZ

Dual N-Channel PowerTrench® MOSFET

20V, 4A, Q1:68mΩ, Q2:100mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 68mΩ at $V_{GS} = 4.5V$, $I_D = 4A$
- Max $r_{DS(on)}$ = 100mΩ at $V_{GS} = 2.5V$, $I_D = 3A$

Q2: N-Channel

- Max $r_{DS(on)}$ = 100mΩ at $V_{GS} = 4.5V$, $I_D = 4A$
- Max $r_{DS(on)}$ = 150mΩ at $V_{GS} = 2.5V$, $I_D = 2A$
- Low gate Charge
- RoHS Compliant

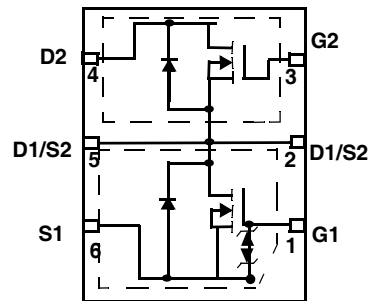
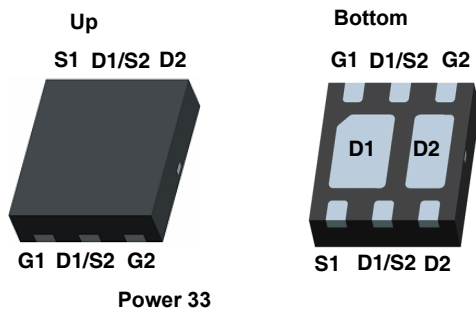


General Description

FDMC6890NZ is a compact single package solution for DC to DC converters with excellent thermal and switching characteristics. Inside the Power 33 package features two N-channel MOSFETs with low on-state resistance and low gate charge to maximize the power conversion and switching efficiency. The Q1 switch also integrates gate protection from unclamped voltage input.

Application

- DC - DC Conversion



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Q1 | Q2 | Units |
|----------------|--|-------------|------|-------|
| V_{DS} | Drain to Source Voltage | 20 | 20 | V |
| V_{GS} | Gate to Source Voltage | ±12 | ±12 | V |
| I_D | -Continuous | 4 | | A |
| | -Pulsed | 10 | | |
| P_D | Power Dissipation (Steady State) Q1 | (Note 1a) | 1.92 | W |
| | Power Dissipation (Steady State) Q2 | | 1.78 | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | | °C |

Thermal Characteristics

| | | | | | |
|-----------------|---|----|-----------|----|------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | Q1 | (Note 1a) | 65 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | Q2 | | 70 | |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|------------|----------|-----------|------------|------------|
| 6890N | FDMC6890NZ | Power 33 | 7inch | 8mm | 3000 units |

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|--------|-----------|-----------------|------|-----|-----|-----|-------|
|--------|-----------|-----------------|------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | | |
|--------------------------------------|---|---|----------|----------|----------|-----------------------|----------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ | Q1 Q2 | 20 20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, referenced to 25°C | Q1 Q2 | | 13 12 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 16\text{V}$, $V_{GS} = 0\text{V}$ | Q1 Q2 | | | 1 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 12\text{V}$, $V_{DS} = 0\text{V}$ | Q1 Q2 | | | ± 10 ± 100 | μA nA |

On Characteristics

| | | | | | | | |
|--|--|---|----------|------------|------------|------------|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ | Q1 Q2 | 0.6 0.6 | 0.9 1.0 | 2 2 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, referenced to 25°C | Q1 Q2 | | -3 -3 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS} = 4.5\text{V}$, $I_D = 4\text{A}$ | Q1 | | 58 77 | 68 100 | m Ω |
| | | $V_{GS} = 2.5\text{V}$, $I_D = 3\text{A}$ | Q2 | | 67 102 | 100 150 | |
| g_{FS} | Forward Transconductance | $V_{DS} = \text{V}$, $I_D = 4\text{A}$ | Q1 Q2 | | 10 7 | | S |

Dynamic Characteristics

| | | | | | | | |
|-----------|------------------------------|--|----------|--|------------|------------|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ | Q1 Q2 | | 205 190 | 270 250 | pF |
| C_{oss} | Output Capacitance | | Q1 Q2 | | 60 60 | 80 80 | pF |
| C_{rss} | Reverse Transfer Capacitance | | Q1 Q2 | | 40 35 | 60 55 | pF |
| R_g | Gate Resistance | $f = 1\text{MHz}$ | Q1 Q2 | | 3.3 2.8 | | Ω |

Switching Characteristics

| | | | | | | | |
|--------------|-------------------------------|---|----------|--|------------|------------|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 10\text{V}$, $I_D = 4\text{A}$, $R_{GEN} = 6\Omega$ | Q1 Q2 | | 4 4 | 10 10 | ns |
| t_r | Rise Time | | Q1 Q2 | | 13 12 | 22 21 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | Q1 Q2 | | 10 7 | 19 14 | ns |
| t_f | Fall Time | | Q1 Q2 | | 6 6 | 12 12 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge at 4.5V | $V_{GS} = 0\text{V}$ to 4.5V | Q1 Q2 | | 2.4 1.8 | 3.4 2.6 | nC |
| $Q_{g(2)}$ | Total Gate Charge at 2V | $V_{DD} = 10\text{V}$ $I_D = 4\text{A}$ | Q1 Q2 | | 1.4 0.6 | 1.9 0.8 | nC |
| Q_{gs} | Gate to Source Gate Charge | | Q1 Q2 | | 0.4 0.5 | | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | Q1 Q2 | | 0.9 0.8 | | nC |

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

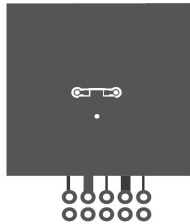
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|--------|-----------|-----------------|------|-----|-----|-----|-------|
|--------|-----------|-----------------|------|-----|-----|-----|-------|

Drain-Source Diode Characteristics

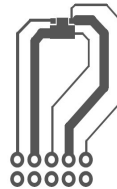
| | | | | | | | |
|----------|---------------------------------------|----------------------------|----------|--|--------------|--------------|----|
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0V, I_S = 4A$ | Q1 Q2 | | 0.94 0.92 | 1.25 1.25 | V |
| t_{rr} | Reverse Recovery Time | $I_F = 4A, di/dt = 100A/s$ | Q1 Q2 | | 18 17 | 27 26 | ns |
| Q_{rr} | Reverse Recovery Charge | | Q1 Q2 | | 9 10 | 14 15 | nC |

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 65°C/W when mounted on a 1 in² pad of 2 oz copper



b. 150°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

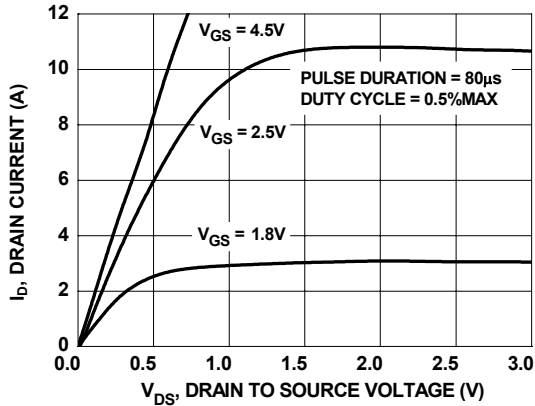


Figure 1. On-Region Characteristics

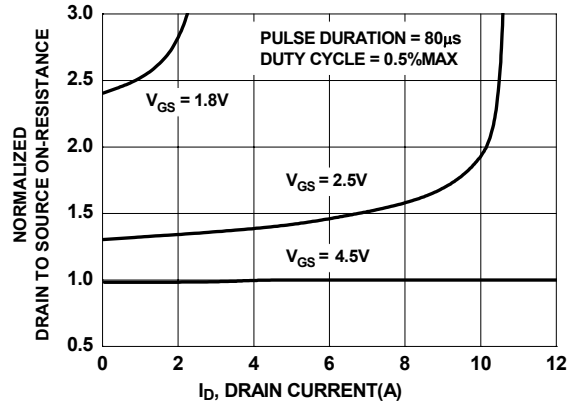


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

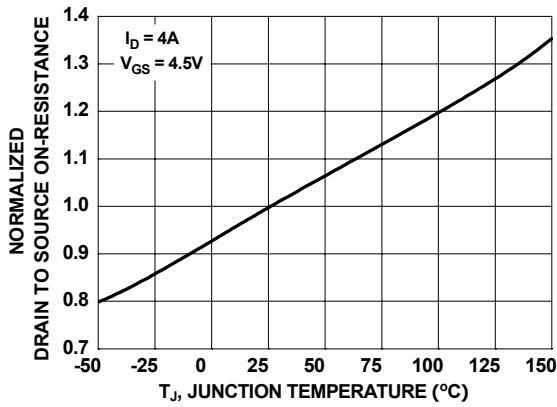


Figure 3. Normalized On-Resistance vs Junction Temperature

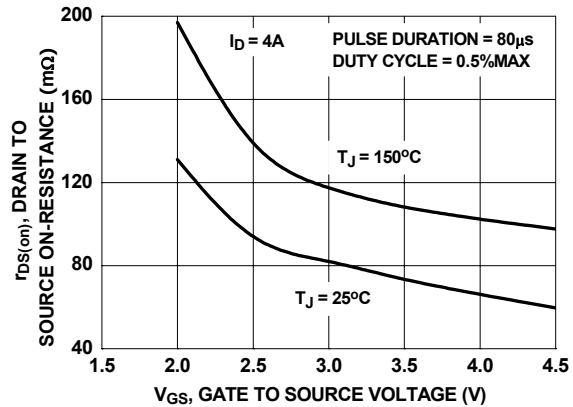


Figure 4. On-Resistance vs Gate to Source Voltage

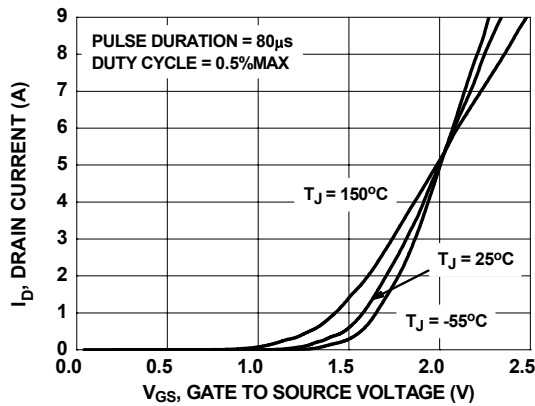


Figure 5. Transfer Characteristics

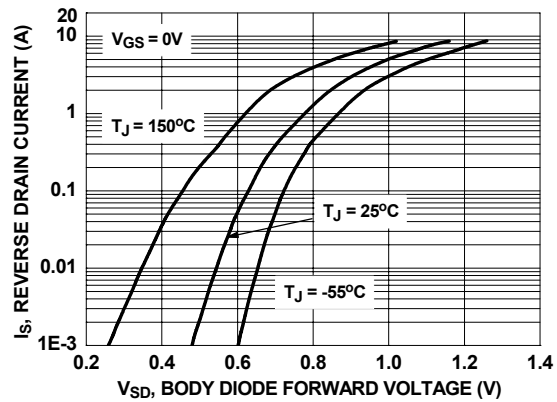


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

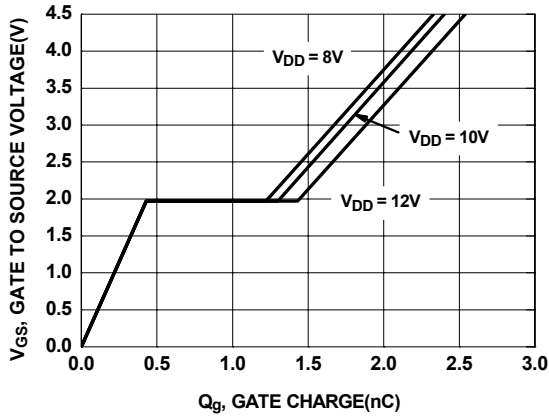


Figure 7. Gate Charge Characteristics

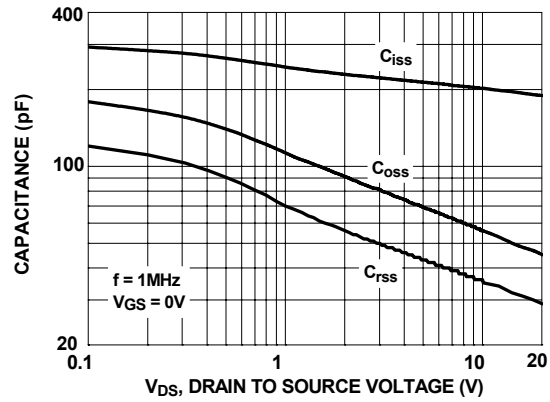


Figure 8. Capacitance vs Drain to Source Voltage

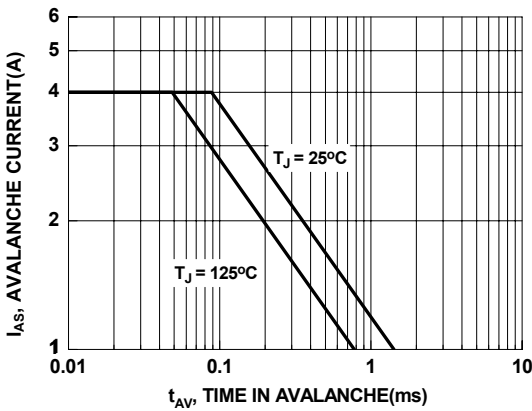


Figure 9. Unclamped Inductive Switching Capability

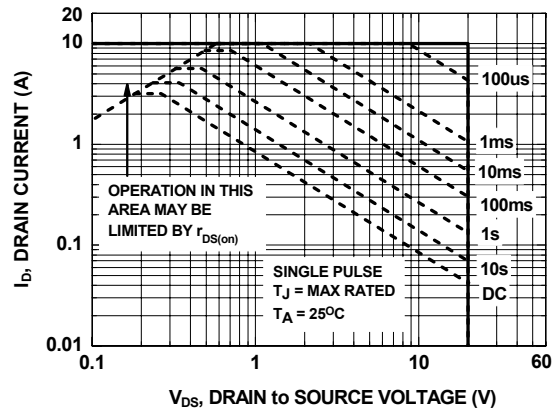


Figure 10. Forward Bias Safe Operating Area

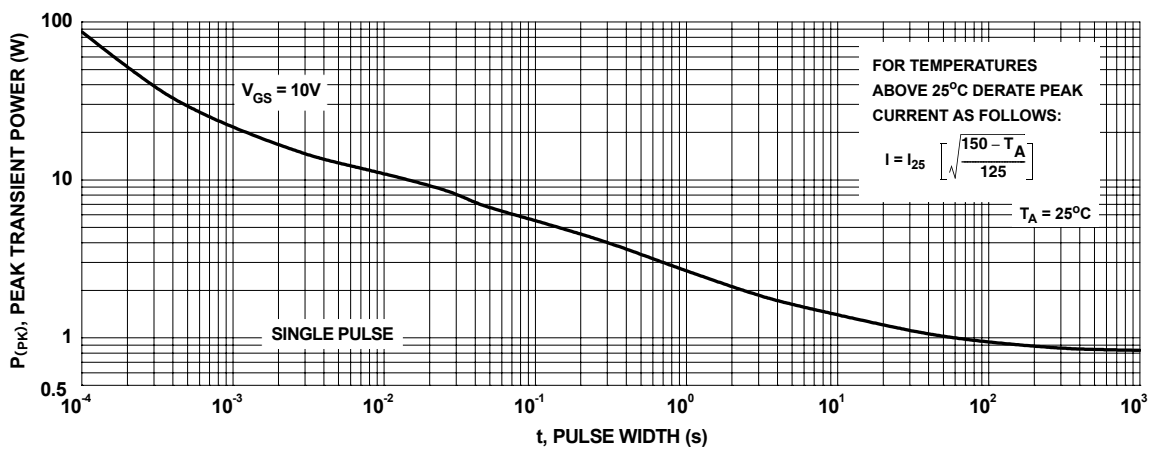


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

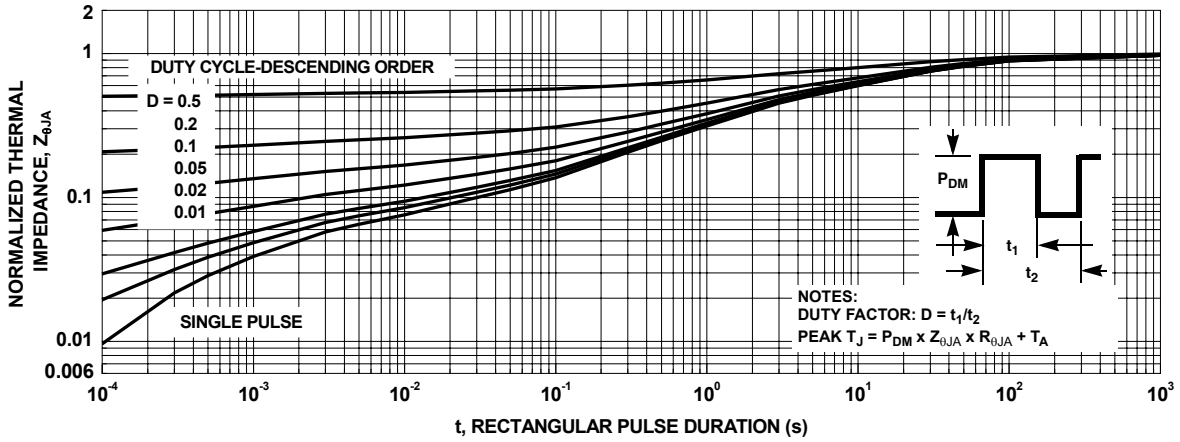


Figure 12. Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel)

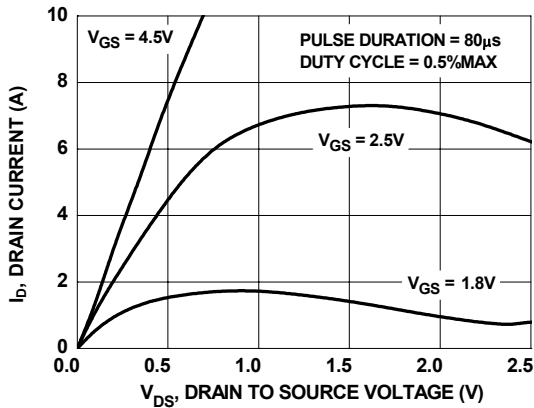


Figure 13. On Region Characteristics

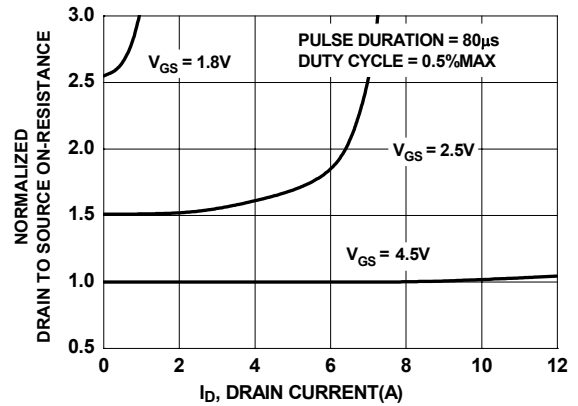


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

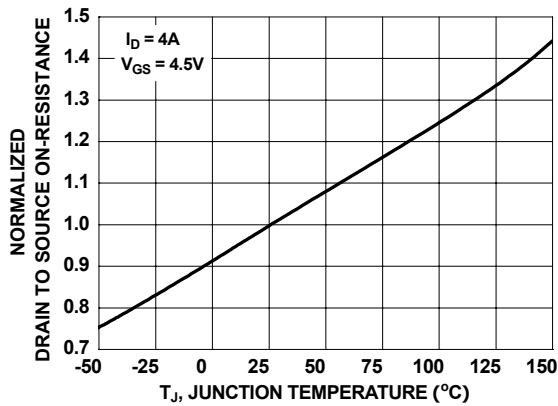


Figure 15. Normalized On Resistance vs Junction Temperature

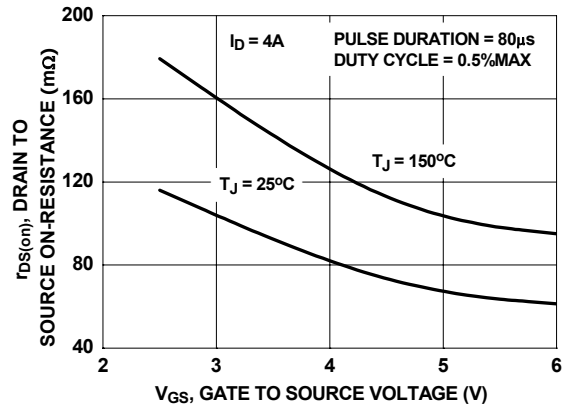


Figure 16. On-Resistance vs Gate to Source Voltage

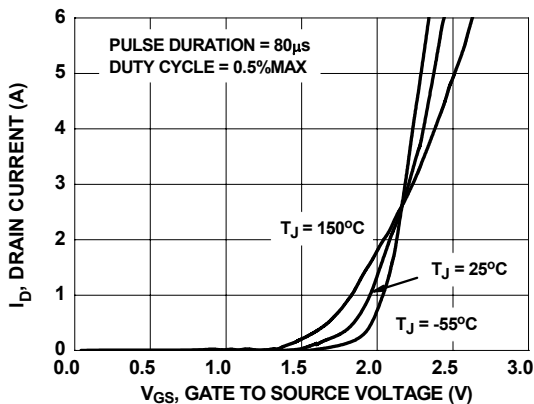


Figure 17. Transfer Characteristics

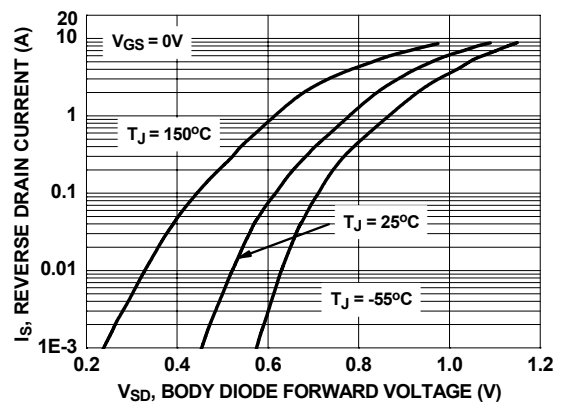


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics

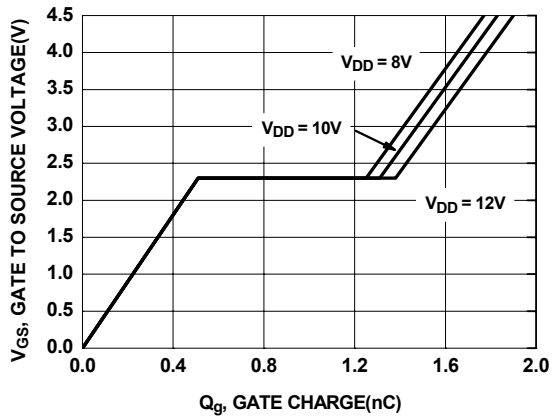


Figure 19. Gate Charge Characteristics

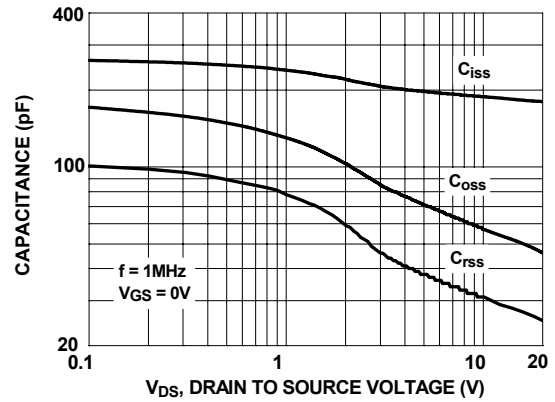


Figure 20. Capacitance vs Drain to Source Voltage

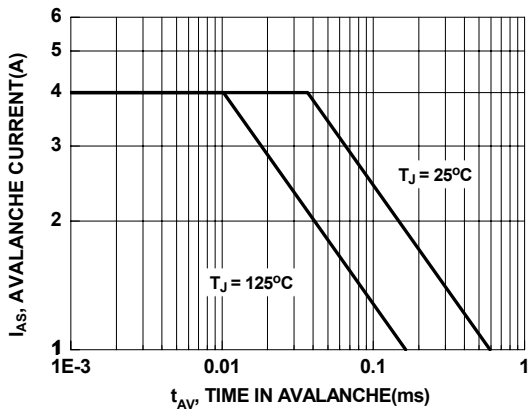


Figure 21. Unclamped Inductive Switching Capability

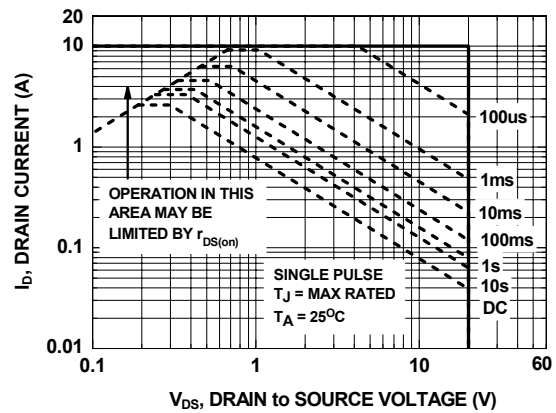


Figure 22. Forward Bias Safe Operating Area

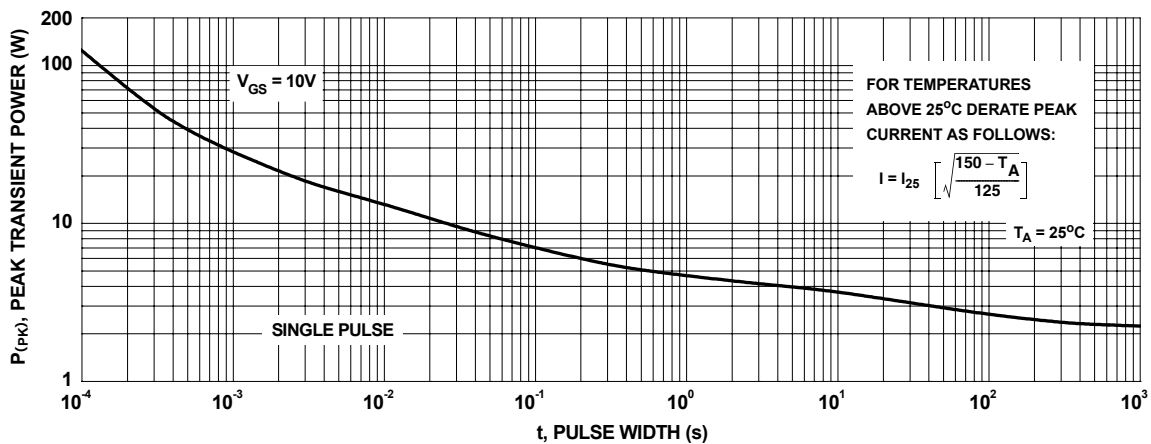


Figure 23. Single Pulse Maximum Power Dissipation

Typical Characteristics

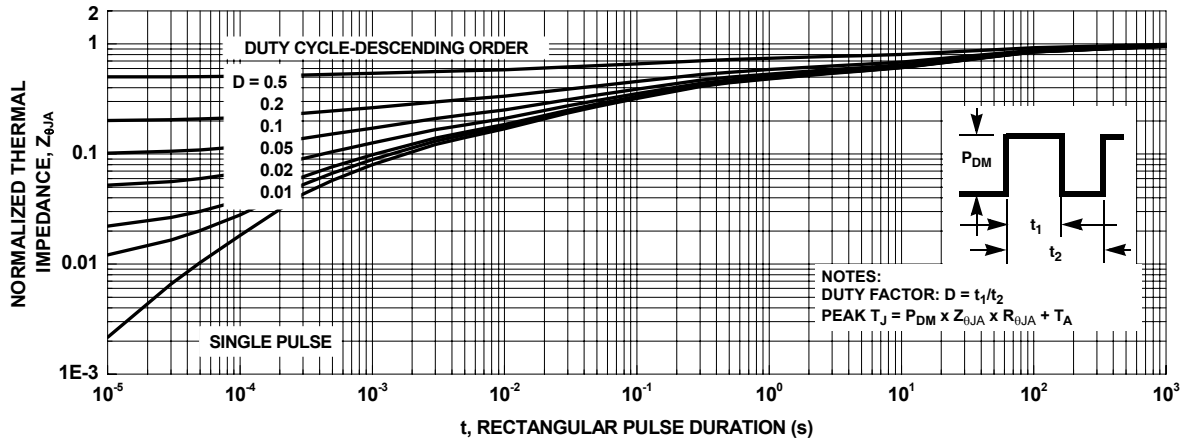
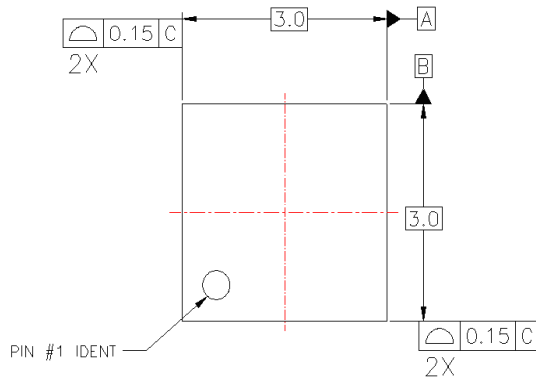
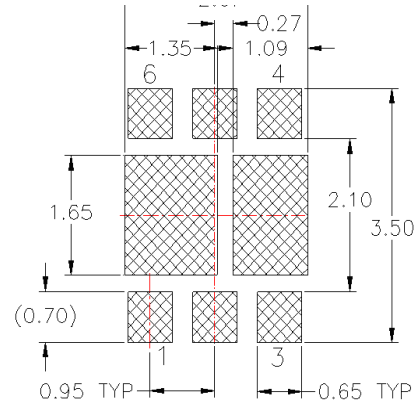


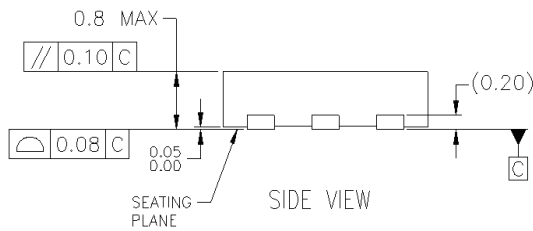
Figure 24. Transient Thermal Response Curve



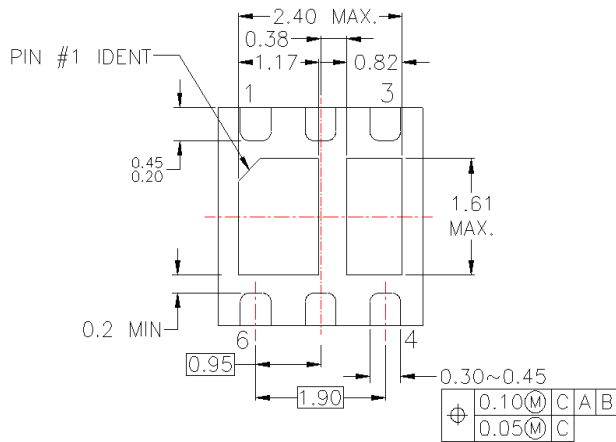
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION WEEA, DATED 11/2001
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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